REMARKS

Claim 1 has been amended. Claims 1 and 2 are pending and under consideration. No new matter is presented in this Amendment. Claim 1 is the independent claim.

DOUBLE PATENTING:

Claims 1 and 2 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14-15 of co-pending application 10/828,326.

Since claims 1 and 2 of the instant application have not yet been indicated as allowable, it is believed that any submission of a Terminal Disclaimer or arguments as to the non-obvious nature of the claims would be premature.

As such, it is respectfully requested that Applicants be allowed to address any provisional obviousness-type double patenting issues remaining once the rejections of claims 1 and 2 under 35 U.S.C. §§102 and 103 are resolved.

REJECTIONS UNDER 35 U.S.C. §102:

Claim 1 is rejected under 35 U.S.C. §102(3) as being anticipated by Ichikawa (U.S. Patent No. 5,901,159).

Independent claim 1 recites a recording/reproducing apparatus comprising: a data scrambler having a random data generator for generating random data in a cycle of 32 KB in order to scramble data having structure of 2 KB for a sector or a data frame and 64 KB for an error correction code (ECC) block.

The Office Action relies on Ichikawa and in particular in column 15, lines 1-30 and column 25, lines 35-50 for the teachings of independent claim 1.

However, a careful review of Ichikawa reveals that the reference does not teach or suggest the novel features recited in independent claim 1.

Ichikawa discloses a digital signal decoder which decodes coded data, for example, a coded digital video signal having error-correcting data such as C_1/C_2 convolutional Reed-

Solomon type data added thereto (abstract).

Ichikawa further discloses that the data is recorded in units of 32Kb data clusters (Fig. 22 and column 13, lines 21-24) and that the data is scrambled by exclusively logically adding together the main data with scramble data generated using as the initial value a value specified by the lower 4 to 7 bits of the physical sector address (column 15, lines 1-5).

In other words, Ichikawa simply discloses recording data in units of 32Kb and scrambling the main data having a structure of 2Kb for a sector.

However, Ishikawa makes no reference or suggestion of generating random data in a cycle of 32Kb, as noted above. Ichikawa at most discloses recording data in units of 32Kb clusters.

Furthermore, Ichikawa makes no reference or suggestion of generating the random data in order to scramble data having a structure of 2Kb for a sector or a data frame and 64Kb for an ECC block. At most, Ichikawa discloses scrambling main data having a structure of 2Kb for a sector (column 13, lines 49-54 and column 15, lines 1-3).

As a matter of fact, nowhere in the specification does Ichikawa disclose scrambling a data having a structure of 64KB for an ECC block.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(b) should be withdrawn because Ichikawa fails to teach or suggest each feature of independent claim 1.

REJECTIONS UNDER 35 U.S.C. §103:

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (U.S. Patent No. 5,901,159), and further in view of Unno (U.S. Patent No. 6,577,642).

Applicants respectfully traverse this rejection for at least the following reason.

Initially it is noted that claim 2 depends from independent claim 1, and as noted above, Ichikawa fails to teach or suggest the novel features of independent claim 1.

Furthermore, it is noted that Unno is relied upon for a teaching of features other than those recited in independent claim 1. Accordingly, Unno fails to cure the deficiencies of Ichikawa.

Finally, Applicants note that Unno is relied upon for a teaching of a random generator comprising a 15-bit serial register r_0 through r_{14} for generating the random data by shifting left synchronized with a clock input for scrambling; and an exclusive OR gate for outputting an exclusive OR value exclusive-ORing output from a higher-most register r_{14} and output from a lower register r_{10} to a lower-most register r_0, wherein the scrambler includes an exclusive OR logic circuit which supplies a result of exclusive-ORing 1-byte input data D_0 through D_7 and each of the 8 outputs of lower registers r_0 through r_7 after left-shifting the 15-bit register r_0 through r_{14} 8 times.

However, a careful review of Unno and the cited passages reveals that Unno does not in fact teach the novel features of claim 2 and thus Applicants respectfully traverse this rejection for at least the following reasons.

Unno discloses a synchronization system and a synchronization method for strict commercial time synchronization by advancing the timing of generation of a PN (Pseudo-random Noise) signal in an upstream station by a transmission line delay.

Unno further discloses in FIG. 4 a block diagram illustrating the configuration of each of the PN generators. Each of the PN generators consists of shift registers of 15 stages 101 to 115 and exclusive-OR circuits 201 to 205. The period of a PN signal generated by each of these PN generators is (2^{15-1}) times the unit bit duration thereof. That is, the period of an output sequence of each of these PN generators is 32767 $(=2^{15-1})$ bits. Thus, each of these PN generators repeatedly outputs a pseudo-random code of the same pattern every period of 32767 bits (column 6, lines 1-8).

Accordingly, although Unno discloses a generator including shift registers and exclusive-OR circuits, Unno does not teach or suggest that the generator performs the scrambling process recited in claim 2.

Therefore, Applicants respectfully assert that dependent claim 2 is allowable at least because of its dependency from claim 1, and because it includes additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claim 2 also distinguishes over the prior art.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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